WHAT IS CLAIMED IS:

1. A demultiplexer for separating desired packets for output from an input digital data which has different format packets multiplexed in a given manner, comprising:

a data input for receiving the input digital data;

a first storage (a shift register) for storing and transferring the input digital data received at the data input;

a second storage (a group of registers) for extracting and storing the headers of the packets from the input digital data stored in the first storage (a shift register);

a calculating unit for analyzing the headers of the packets stored in the second storage (a group of registers);

an output destination determining unit for determining the destination of the packets from a packet identifier which is contained in the headers of the packets stored in the second storage (a group of registers);

a separator arranged responsive to a result of the calculating action of the calculating unit and an output of the output destination determining unit for separating the desired packets from the input digital data received from the first storage (a shift register);

a command memory for storing micro-codes provided for selecting a controlling action in each multiplexing format;

a counter for determining an execution address of the micro-code stored in the command memory;

a controller for controlling the action of each component with the micro-code read out from the command memory by the execution address determined by the counter; and

a system clock controller for extracting the timing data from the input digital data stored in the first storage (a shift register) and controlling a system clock with the timing data.

2. A demultiplexer according to claim 1, wherein the output destination determining unit is a contents addressable memory.

3. A demultiplexer according to claim 1, further comprising a data writing means for writing data for determining the destination in a built-in memory of the output destination determining unit.

4. A demultiplexer according to claim 1, wherein the second storage (a group of registers) includes a register acting as a counter for managing the length of each packet multiplexed in the input digital data.

5. A demultiplexer according to claim 1, wherein the calculating unit is an arithmetic logic unit.

6. A demultiplexer according to claim 1, wherein the calculating unit includes a dedicated circuit for detecting the continuity between packets in the input digital data.

7. A demultiplexer according to claim 1, wherein the calculating unit includes a dedicated circuit for subjecting the head of each packet in the input digital data to a bit manipulating process and storing it in the second storage (a group of registers).

8. A demultiplexer according to claim 1, wherein the controller generates from the micro-code read out from the command memory a control signal for actuating one or more components at one time.

9. A demultiplexer according to claim 1, wherein the data input includes an input buffer for temporarily saving the input digital data.

10. A demultiplexer according to claim 9, wherein the input buffer when receiving the input digital data has a data read out in synchronism with the shifting action of the first storage (a shifter register).

11. A demultiplexer according to claim 1, wherein the destination comprises a plurality of buffer memories for storing the packets separated by the separator.

12. A demultiplexer according to claim 1, wherein the destination is a single buffer memory which has an array of storage regions for storing the packets respectively separated by the separator.

13. A demultiplexer according to claim 1, wherein the separator includes a means for modifying the byte endian.

14. A demultiplexer according to claim 1, further comprising:

a data writing means for writing the micro-codes in the command memory.